REMARKS

Reconsideration of the application in view of the above amendments and the following remarks are respectfully requested.

Claims 1-13 and 15-20 are currently pending in this application. Claims 1 and 2 are rejected under 35 U.S.C. §103(a) as being unpatentable over Costello et al. (U.S. Patent 6,754,894) in view of Brown, III et al. (U.S. Patent 6,038,636). Claims 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Costello et al. in view of Brown, III et al. and Niiyama et al. (U.S. Patent 5,400,389).

It is gratefully acknowledged that Claims 11-13 and 15-20 have been allowed and Claims 6-10 have been objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims.

Costello teaches one Random Access Memory (RAM) and two flash memories as shown in Fig. 5. However, the present application, as recited by the Claims, is drawn to a device which uses two RAMs and one flash memory. In other words, unlike Costello, the present application, as recited by the Claims, is drawn to a device which uses first and second RAMs for providing an operation area to store execute program data and temporary data; accordingly, a large capacity memory device is not necessary.

Furthermore, the present application, as recited by the Claims, is drawn to a device which copies the program data from the flash memory to the first RAM. Conversely, Costello teaches copying application software from a NAND flash memory (512) to a NOR flash memory (508) (e.g., see, Cosetello, Col. 7, Lines 28-29). By storing the application software in the NOR flash memory (508) as shown in Fig. 5, Costello, unlike the present application, requires a large capacity memory. Accordingly, the NOR flash memory (508) of Costello cannot be properly substituted for the first and second RAMs, as recited by the Claims of the present application.

Brown, III discloses a method and apparatus for reclaiming and defragmenting a flash memory device, which does not cure the shortcomings of Costello as described herein.

Notwithstanding, independent Claim 1 has been amended, as set forth above herein, to include the recitation of a first Random Access Memory (RAM) for providing an operation area to store and execute the copied program data; and a second RAM for storing data generated during the execution of program data, wherein the first and second RAMs are independent memories, which is neither taught nor suggested by either Costello et al. or Brown III. As such, amended independent Claim 1 is believed to be in condition for allowance.

Without conceding the patentability of dependent Claims 2-10, per se, these claims are believed to be patentable over the combination of Costello and Brown, III, based on their respective dependency from amended independent Claim 1.

Accordingly, Claims 1-10 as now presented, as well as previously allowed Claims 11-13 and 15-20, are believed to be in condition for allowance. Should the Examiner believe that a telephone conference or personal interview would facilitate resolution of any remaining matters, the Examiner may contact Applicant's attorney at the number given below.

Respectfully submitted,

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